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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/589,722	08/17/2006	Shoji Kawahito	292765US2PCT	2222
22850	7590	05/02/2008		
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314				
EXAMINER				
EFTKHAZADEH, ARDESHIR				
ART UNIT		PAPER NUMBER		
2815				
NOTIFICATION DATE		DELIVERY MODE		
05/02/2008		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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# Office Action Summary

## Application No.

10/589,722

## Applicant(s)

KAWAHITO, SHOJI

## Examiner

ARDESHIR EFTEKHARZADEH

## Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 24 March 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) 2,4,6,9-11 and 13 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3,5,7,8 and 12 is/are rejected.
- 7) ☒ Claim(s) 7 and 8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB008)  
Paper No(s)/Mail Date 11/17/2008.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application.
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED OFFICE ACTION

### **Claim Rejections - 35 U.S.C. § 112**

- (1) The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

- (2) **Claims 7 and 8** are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter Applicant regards as the invention.

- (3) With respect to claim 7: claim 7 recites that the photo-gate electrodes are made from the same material that a MOS transistor in a CMOS integrated circuit. A MOS transistor in a CMOS integrated circuit can be made from a variety of materials. Since there is no universally accepted material for any MOS transistor, it is not clear what the applicant intends to exclude others from making and using.

- (4) With respect to claim 8: The term "low" in claim 8, line 2 is a relative term which renders the claim indefinite. The term "low" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

### **Claim Rejections - 35 USC § 103**

- (5) The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

- (6) **Claims 1, 5, 7, 8 and 12** are rejected under 35 U.S.C. § 103(a) as being unpatentable over Takayanagi et al, US patent publication No. 6,396,570, henceforth referred to as Takayanagi, in view of Ahrenkeil, US patent publication no. 4,165,471, henceforth referred to as Ahrenkeil.

(7) With respect to claim 1:

Takayanagi discloses a time-of flight range-finding sensor (title and abstract) comprising: an insulator layer formed on a semiconductor substrate (see for example, Fig. 4 and notice that there must be layer between the gate electrodes 5 and 5 and the substrate to isolate the gates from the substrate); two conductive photo-gate electrodes disposed close to each other, being transparent for a wavelength of a light reflected by the target object (see for example, 5 and 6, Fig. 4). Takayanagi does not seem to explicitly disclose the gates to be transparent, however Ahrenkeil discloses that transparent gates material would make the sensor more sensitive (col. 2, lines 46-47). Takayanagi disclose first floating diffusion layers disposed under and at ends of the photo-gate electrodes (see for example, n regions, Fig. 4), wherein regions of the semiconductor substrate beneath the two photo-gate electrodes and beneath a gap between the two photo-gate electrodes are used as a photodetector layer (a recitation of intended use of the substrate, although nevertheless met by the cited prior art). As it was discussed above, it would have been obvious to make the electrodes from transparent material as taught by Ahrenkeil to increase sensitivity.

(8) With respect to claim 5:

Since the difference between a field oxide and a gate oxide is the manufacturing process of the oxide layer, the "field oxide" recitation is a product by process limitation and does not distinguish the claimed invention from the cited prior art.

(9) With respect to claim 7:

MOS transistors gate materials can be one of variety of materials. The only property of such a material is electrical conductivity. The precise type of material of gates 5 and 6 is not explicitly disclosed in Takayanagi, but there is no doubt that the material is taught to be conductive. The limitation is met nevertheless.

(10) With respect to claim 8:

The claim recites "both a p-type well and an n-type well are not formed in the semiconductor substrate." This is understood as a negative limitation that excludes a configuration in which both a p-type well and an n-type well are formed in semiconductor substrate. Takayanagi discloses a device in which there is no recitation or disclosure with regard to a p-type well. No where in the disclosure of Takayanagi is there a mention of a p-type

well. Therefore Takayanagi discloses a device in which both a p-type well and an n-type well are not formed in the semiconductor substrate and meets this limitation. The substrate disclosed in Takayanagi utilizes a layer with p-type doping, which is low compare to a p<sup>+</sup> concentration doping and therefore meets this aspect of limitation also.

(11) With respect to claim 12:

The recitation “wherein range information is obtained from the ratio of two signals taken out respectively from the photo-gate electrodes, while intensity information is obtained from the sum of the two signals” is a recitation of intended use of the device. Not only does it not limit the scope of the claimed invention, it does not patentably distinguish the claimed invention from the cited prior art either.

(12) **Claim 5** is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takayanagi et al, US patent publication No. 6,396,570, henceforth referred to as Takayanagi, in view of Bellutti et al, Microelectronic Reliability 39, (1999) 181-185, henceforth referred to as Bellutti.

(13) With respect to claim 5:

Takayanagi does not appear to explicitly disclose a field oxide being utilized as the gate oxide, however, Bellutti discloses a transistor which a field oxide used as gate oxide, (Fig. 1, Bellutti) and teaches that such a field oxide would be more reliable (abstract). Therefore to increase reliability it would have been obvious to utilize a field oxide in place of a gate oxide.

(14) **Claim 3** is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takayanagi et al, US patent publication No. 6,396,570, henceforth referred to as Takayanagi, in view of Suzuki et al, US patent publication no. 4,136,292, henceforth referred to as Suzuki.

(15) With respect to claim 3:

Takayanagi discloses first and second signal read out circuits (see for example, elements 7 and 8, and also col. 6, lines 35-50). Takayanagi does not appear to explicitly disclose first MOS transistors, with their gates coupled to diffusion layers since it does not disclose with the internal circuitry of the disclosed reading circuits or subsequent circuits are. Nevertheless it is abundantly clear that the diffusion regions collect photo electrically generated charges that provide potential and therefore, the device disclosed by Takayanagi is ready to be improved by providing further details for the circuitry.

Art Unit: 2815

Suzuki provides just such a detail; with the predictable result of reading the signal input provided by Takayanagi. Suzuki discloses two data lines (Fig. 1, L1 and L2), ready to be coupled to any two sources of data signals coupled to two MOS transistors (Fig. 1, 12 and 13). Therefore it would have been obvious to substitute the two first and second reading circuits disclosed by Takayanagi, by the two transistors disclosed by Suzuki and to that end, couple the two transistors to the two data lines disclosed by Suzuki for obtaining the predictable result of reading the signals provided by Takayanagi.

### **Conclusion**

- (16) A shortened statutory period for reply to this Office Action is set to expire **THREE MONTH** from the mailing date of this Office Action. Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ardeshtir Eftekharzadeh whose telephone number is (571) 270-3262. The examiner can normally be reached on Monday-Thursday 10:30 AM-9:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://portal.uspto.gov/external/portal/pair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. E./

*Examiner, Art Unit 2815*